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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/676,597	10/01/2003	Peter Beer	W&B-INF-1951	7989

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EXAMINER	
YOHA, CONNIE C	

ART UNIT	PAPER NUMBER
2827	

DATE MAILED: 11/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/676,597	BEER, PETER
	Examiner	Art Unit
	Connie C. Yoha	2827

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Connie C. Yoha

CONNIE C. YOHA
PRIMARY EXAMINER

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office acknowledges receipt of the following items from the Applicant:

Papers submitted under 35 U.S.C. 119(a)-(d) have been placed of record in the file.

2. Claims 1-7 are presented for examination.

Claim Rejections - 35 USC э 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Nakashima, Pat. No. 5351213.

With regard to claim 1, Nakashima discloses a memory circuit comprising: a memory cell array (fig. 4, 4) including a plurality of word lines (fig. 4, WL) and a plurality of bit lines (fig. 4, BL, /BL) for addressing said plurality of memory cells, said memory cells disposed at crossover points of said word lines with said bit lines (fig. 4, 4); a plurality of write amplifiers (fig. 4, sense amp.1, sense amp.2) each one of said plurality of write amplifiers assigned to a group of said plurality of bit lines (fig. 4, BL, /BL); and an address decoding circuit (fig. 4, 5, 5' col. Decoder) for simultaneously activating a group of said plurality of write amplifiers, depending on a test mode signal, so that said

group of said plurality of write amplifiers writes a test datum to a group of said plurality of memory cells via respectively assigned ones of the plurality of bit line (col. 5, line 35-60).

With regard to claim 2, Nakashima discloses memory circuit further comprising: a plurality of switching devices (fig. 4, 11, 12) each of one of said plurality of write amplifiers connected to assigned ones of said plurality of bit lines via a respective one of said plurality of switching devices in order to write the test datum from an activated one of said plurality of write amplifiers to an addressed memory cell via one of the plurality of bit lines addressed by a write address (col. 5, line 41-43, 51-60).

With regard to claim 3, Nakashima discloses wherein said address decoding circuit is configured to simultaneously connect one of said plurality of write amplifiers to assigned ones of said plurality of bit lines depending on the test mode signal (col. 5, line 43-60).

With regard to claim 7, Nakashima discloses a memory circuit comprising: a memory cell array (fig. 4, 4) including a plurality of word lines (fig. 4, WL) and a plurality of bit lines (fig. 4, BL, /BL) for addressing said plurality of memory cells; a plurality of write amplifiers (fig. 4, sense amp.1, sense amp.2) each one of said plurality of write amplifiers assigned to a group of said plurality of bit lines (fig. 4, BL, /BL); and an address decoding circuit (fig. 4, 5, 5' col. Decoder) for simultaneously activating a group of said plurality of write amplifiers, depending on a test mode signal, so that said group of said plurality of write amplifiers writes a test datum to a group of said plurality of memory cells via respectively assigned ones of the plurality of bit line (col. 5, line 35-

60); a plurality of switching devices (fig. 4, 11, 12) each of one of said plurality of write amplifiers connected to assigned ones of said plurality of bit lines via a respective one of said plurality of switching devices in order to write the test datum from an activated one of said plurality of write amplifiers to an addressed memory cell via one of the plurality of bit lines addressed by a write address (col. 5, line 41-43, 51-60); and column select lines (fig. 4, the line runs between switch 1 or 12 through the col. Decoder 5, 5') connect between said address decoding circuit (fig. 4, col. Decoder 5, 5') and said switching devices (fig. 4, 11 or 12), said address decoding circuit activating selected ones of said switching devices in dependence on the test mode signal (fig. 4, TE) (col. 5, line 51-60).

Drafted as Method claim

4. As per claim 4-6 encompass the same scope of invention as to that of claim 1-3 except they draft in method format instead of apparatus format. The claim is therefore rejected for the same reason as set forth above.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicants' disclosure. Kikutake et al (6643805), Nakano et al (6515920) and Kikuda (5903575) disclose a memory device having testing operation.

6. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

7. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see MPEP 710.02 (b)).

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to whose telephone number is (571) 272-1799. The examiner can normally be reached on Mon. - Fri. from 8:00 A.M. to 5:30 PM. The examiner's supervisor, David Nelms, can be reached at (571) 272-1787. The fax phone number for this Group is (703) 872-9306. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-0956.

9. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov should you have questions on access to the Private Pair system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

C. Yoha

November 2005

CONNIE C. YOHA
PRIMARY EXAMINER